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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/970,297	10/02/2001	Sean S. Chen	NSC-P05052	9656

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EXAMINER	
HILTUNEN, THOMAS J	

ART UNIT	PAPER NUMBER
2816	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

TH

Office Action Summary	Application No.	Applicant(s)	
	09/970,297	CHEN, SEAN S.	
	Examiner	Art Unit	
	Thomas J. Hiltunen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7,8,12,13,16-21 and 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7,8,12,13,16-21 and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 July 2007* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Applicant's request for continued examination has filed 19 July 2007 has been received. The amendment received 19 July 2007 has been entered and considered below responsive to applicant request for continued examination.

Drawings

Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "emitter follower for the emitters of said plurality of transistor" and "a voltage pull up device implemented as a first transistor" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Additionally, figure 3 fails to show any of the detail or include a text label of circuit 320 as recited in the specification. Furthermore 320 of Fig. 3 discloses a blank, non-descriptive, box. Such detailed drawings or text labels are critical for examiners who need to quickly search and review thousands of patent documents on a daily basis, and without such drawings or text labels the examiners would have much difficulty performing such a task.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure

number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance..

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-4, 7, 8, 12, 13, 16-21 and 23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claims 1, 7 and 16, the recitation of "first ("second" with respect to claim 1) transistor operable as an emitter follower of the emitters of said plurality of transistors" is misdescriptive. As far as understood transistor 309 of Fig. 3 of the instant application refers to "an emitter follower" transistor and "the plurality of transistors" refers to the transistors composing the band-gap reference circuit (i.e., 201-207 of Fig. 3 of the instant application). As can be seen, the emitter follower 309 does not follow the

emitter of the all of the plurality of transistors of the band-gap reference unit 201-207. For instance, 206 and 207 do not have an "emitter" since they are MOS transistors, additionally 309 does not follow the emitters of transistors 201 and 202. Furthermore, the recitation of "the output voltage" on line 14 of claim 7 lacks antecedent basis.

With respect to claims 13 and 21, it is not understood if "a voltage-up device" as recited on line 2 refers to the recited pull-up device as claims 7 and 16.

With respect to claim 16, the recitation of "the band-gap reference voltage" on line 3 lacks antecedent basis.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 7, 8, 12, 13 and 16-21 rejected under 35 U.S.C. 102(b) as being anticipated by Kadanka et al. (USPN 5,920,184).

With respect to claims 1, 7 and 16, as far as understood, Kadanka et al. discloses in Fig. 2, "an electronic device (circuit of Fig. 2), comprising:

a silicon substrate (the circuit of Fig. 2 is implemented on a silicon substrate, see Col. 2 lines 46-48. Furthermore, the circuit of Fig. 2 is implemented in a semiconductor device on a chip that includes other "complex circuits and systems", see Col. 1 lines 11-12 and 28-30);

electronic circuitry constructed in said silicon substrate (the circuit of Fig. 2 controls an electronic device that receives the band-gap voltage output and composed on the same chip, i.e., same silicon substrate, again see Col. 1 lines 11-12 and 28-30); and

a band-gap reference circuit comprising (electronic circuit of Fig. 2 is a band-gap reference circuit):

a band gap reference unit comprising a plurality of transistors (42 with Q9B, R3 and Qa of 44, which generate a band gap voltage at node 75, see Col 2 lines 37-44),

a buffer circuit (Q22),

a voltage pull-up device electronically coupled in said electronic device (Q15), and

a first transistor operable as an emitter follower for the emitters of said plurality of transistors (Qc), wherein the emitter of said first transistor is electrically coupled to said buffer circuit via said voltage pull-up device (the emitter of QC is coupled to the base of Q22 via the base to collector connection of pull-up device Q15), wherein said first transistor and said voltage pull-up device in combination pull the VBE of said buffer circuit toward Vcc (the output of the collector of Q15, which is controlled by the emitter current of QC, pulls the base voltage of Q22 up toward Vcc, thus pulling the base to emitter voltage, i.e., VBE, of Q22 toward Vcc);

wherein said electronic circuitry requires reference to the output voltage of said band-gap reference circuit (the electronic circuits and systems receives the output of Fig. 2), wherein said buffer circuit comprises a second transistor (Q22), and wherein said single component voltage pull-up device is coupled between said band-gap

reference unit and said buffer circuit (Q15 is coupled between node 75 and the base of transistor Q22).

With respect to claims 2, 8 and 17, Kadanka et al. discloses, the electronic device being composed in a chip (i.e., integrated circuit).

With respect to claim 3, Kadanka et al. discloses the circuit of Fig. 2 is implemented on a silicon substrate, see Col. 2 lines 46-48.

With respect to claims 12 and 20, Kadanka et al. discloses that Vcc is a low supply voltage.

With respect to claims 13 and 21, as far as understood, Kadanka et al. discloses enabling the low supply voltages by Q15.

With respect to claims 4 and 18, Kadanka et al. discloses that the buffer is implemented as a transistor Q22.

With respect to claim 19, Kadanka et al. discloses Q22 being an emitter follower in that Q22 follows the emitter current of QC.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kadanka et al. (USPN 5,9220,184) in view of Mietus (USPN 5,666,046).

Kadanka et al. does not expressly disclose that transistor Q22 (i.e., transistor which provides the band-gap voltage, and the emitter follow buffer) has a "less than 1.0 V_{BE}". However, it is notoriously well-known, as expressly taught by Mietus (e.g., see Col. 1, lines 56-67), to use transistors that have a V_{BE} voltage of 0.7 volts in a band-gap circuit for the advantage of using a lower supply voltage (e.g., 0.8 volts). Therefore, it would have been obvious for one skilled in the art to manufacture all of the transistors of Kadanka et al. (including transistor Q22) with "less than 1.0 V_{BE}" for the expected advantage allowing for a lower supply voltage. One would have been motivated to manufacture all of the transistors of Kadanka et al. (including transistor Q22) with "less than 1.0 V_{BE}" to lower the supply voltage thus reducing the amount of power consumed by the circuit of Fig. 2 of Kadanka et al.

Response to Arguments

Applicant's arguments with respect to claims 1-4, 7, 8,12, 13,16-21 and 23 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571)272-5525. The examiner can normally be reached on M-F 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards, can be reached on (571)272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kenneth B. Wells/
Primary Examiner
Art Unit 2816

TH
September 12, 2007